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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : G06F 15/78 — A1

(11) International Publication Number: WO 97/49042

(43) International Publication Date: 24 December 1997 (24.12.97)

(21) International Application Number: PCT/US97/10763

(22) International Filing Date: 20 June 1997 (20.06.97)

(30) Priority Data:
60/020,249 21 June 1996 (21.06.96) US

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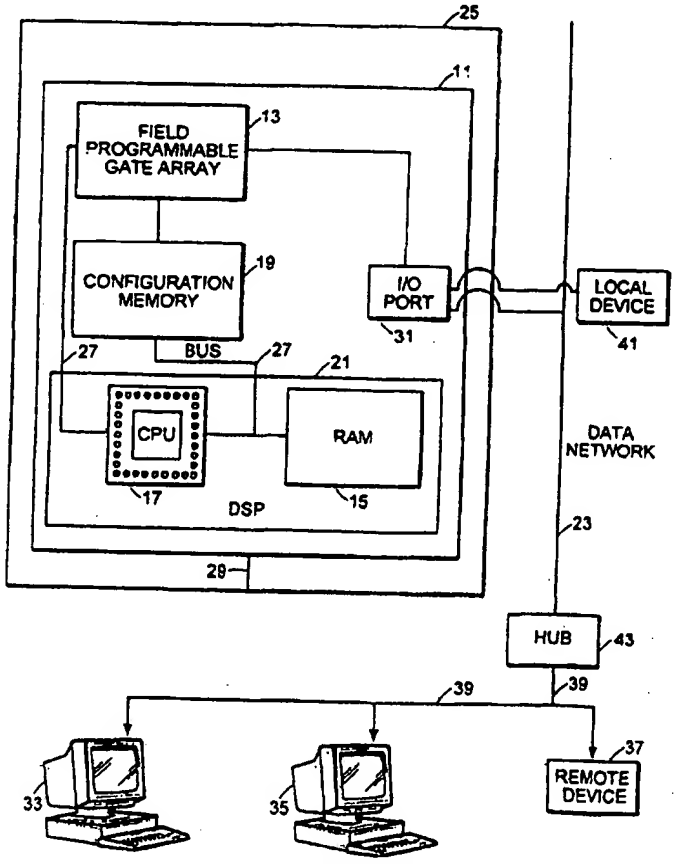
(81) Designated States: JP, European patent (AT, BE, CH, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: DYNAMICALLY RECONFIGURABLE HARDWARE SYSTEM FOR REAL-TIME CONTROL OF PROCESSES

(57) Abstract

A dynamically reconfigurable hardware system provides real-time control of an external device. The system has a configuration memory (19), a reconfigurable logic module (13) and a processor (17), and a communication port (31). The configuration memory (19) stores a hardware configuration of the reconfigurable logic module (13). The reconfigurable logic module (13) in communication with the configuration memory (19), establishes the hardware configuration in the module (13) on receipt of a configuration signal. The processor (17) is in communication over a data bus (27) with the reconfigurable logic module (13), the configuration memory (19), and sends the configuration signal to the reconfigurable logic module (13) and establishes the hardware configuration in the configuration memory (19). The communication port (31), coupled to the reconfigurable logic module (13) independently of signals on the data bus (27), controls the external device.



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Dynamically Reconfigurable Hardware System for Real-Time Control of Processes

DESCRIPTION

Technical Field

This invention relates to virtual computing environments utilizing reconfigurable logic modules, such as gate arrays and the real-time control of external devices..

Background Art

Although there can be many different implementations of virtual computing devices which make use of field programmable gate arrays ("FPGAs") an example of a prior art version of such system is US patent 5,497,498. FPGAs are discussed in Villasenor and Mangione-Smith "Configurable Computing", Scientific American, June, 1997, pages 67-71. These references are incorporated herein by reference.

A recent trend in factory automation is to replace dedicated and proprietary computers within the factory with an open architecture control system based on general purpose personal computers (PC). Major control vendors now have business plans at least partially impacted by the PC. Some major control equipment suppliers are already pursuing strategies based entirely on PC control. Towards facilitating the transition from specialized computers to general purpose computers, the Open Modular Architecture for Control (OMAC) specification was developed and adopted by several major corporations.

Maintaining compatibility with the past standards, however, is very important. Consequently, previous attempts to improve control systems while maintaining full compatibility has resulted in relatively minor improvements. Of special note are attempts to replace prior networking schemes for distributing real-time control with methods designed to operate on the general purpose PCs. With the specialized hardware, real-time control was feasible since a dedicated machine had little overhead beyond simply functioning as it was designed to do. That is, network-distributed real-time control requires fast hardware and a fast communications link in order to effectively control devices in real-time. In the prior art, such real-time control was feasible due to the dedicated nature of the equipment. So long as the dedicated system could process the data quickly enough, and perform as designed, then real-

time control worked.

When using generic PCs as the controlling computer, it must be assured that the system can still maintain network-distributed real-time control. Current prior art attempts have been unable to manage effective network-distributed real-time control. The reason is that the bandwidth of the physical layer on which the prior art systems rely is too slow due to their relying on communication over the host computer's internal I/O bus.

Summary Of the Invention

The present invention supplies a solution to the need for allowing network-distributed real-time control and also allows the controller to be dynamically reconfigurable in real-time in response to input received from a controlled device that is linked to the controller. Configuration occurs parallel to and in a manner independent of the host computer's processor.

In a preferred embodiment of the invention is provided a dynamically reconfigurable hardware system for real-time control of an external device. The system has a configuration memory, a reconfigurable logic module and a controller, and a communication port. The configuration memory is for storing a hardware configuration of the reconfigurable logic module. The reconfigurable logic module in communication with the configuration memory, establishes the hardware configuration in the module on receipt of a configuration signal. The controller is in communication over a data bus with the reconfigurable logic module, the configuration memory, and sends the configuration signal to the reconfigurable logic module and establishes the hardware configuration in the configuration memory. The communication port, coupled to the reconfigurable logic module independently of signals on the data bus, controls the external device because the communication port is coupled to the reconfigurable logic module, a device may be controlled in real-time in parallel to and in a manner independent of a processor within a host computer. The term "reconfigurable logic module", as used in this description and the following claims, means any digital processing module having a hardware configuration that is field programmable, such as a field programmable gate array (FPGA) or a system programmable gate array (SPGA).

In a further embodiment of the invention the data bus is in communication with a network, such as the Internet, allowing receipt of hardware configuration data from remote networked locations. In further embodiment, the configuration memory may be dual-ported

random access memory or electronically erasable programmable read-only memory. In another related embodiment, the controller is in communication with a network, and at least a portion of the hardware configuration is referable from a remote location on the network. In a still further embodiment, the system also has a computer having a central processing unit in communication with the data bus, a graphics display for a user interface, and a process executing on the central processing unit that send user interface data to the display, wherein the reconfigurable logic module performs computations in parallel with the process executing on the central processing unit. The network may be the Internet, the user interface may be an Internet browser, and the browser retrieves the hardware configuration, or a part of such configuration, through the Internet. The system may also include a digital signal processor that includes the controller. The network may utilize the IEEE P1394 protocol.

In a related method according to an employment of the present invention, there are provided the steps of (a) storing hardware configuration in a configuration memory; (b) providing a reconfigurable logic-module in communication with the configuration in the module; (c) establishing the hardware configuration in the reconfigurable logic module; and (d) utilizing the reconfigurable logic module to control an external device in real time. In a further embodiment, step (c) includes providing at least a portion of the hardware configuration to the reconfigurable logic module over a network.

Brief Description of the Drawings

The foregoing invention will be more readily understood by reference to the following detailed description, taken with the accompanying drawing, in which FIG. 1 is a block diagram of a preferred embodiment of the invention.

Detailed Description of Specific Embodiments

A preferred embodiment of the invention embraces the Open Modular Architecture for Control specification, through installing the invention within host PC systems, with communications between the invention and the host computer performed through the computer's data bus. To overcome the bandwidth concerns of the prior art systems, the embodiment avoids using the host computer's I/O sub-system, removing from the host's I/O sub-system the strain of supporting a protocol-intensive application as demanding as real-time control. In addition, by avoiding the host computer's I/O sub-system, the embodiment is

insulated from interrupts generated by other processes running on the host, interrupts that could interfere with critical real-time control operations. The embodiment utilizes a dedicated I/O port for connecting to a device to be controlled, thus preventing the unpredictable performance inherent in using the host computer's I/O sub-system.

The embodiment also implements an optimized communication protocol adapted to controlling applications under critical hard real-time constraints, allowing for high-precision, high-bandwidth real-time distributed computation and control. High-precision is provided through use of 16 bit analog-to-digital (A/D) and digital-to-analog (D/A) conversion based upon 18-bit calibration, instead of the more common 12-bit to 14-bit A/D-D/A conversion. In a preferred embodiment communication protocol will preferably be implemented over a control network capable of sustaining a data transfer rate of at least 200 Megabits per second (Mbits/sec), to allow for coupling real-time control with transmission of video signals or high-density graphics images.

The embodiments of the invention are designed to allow control of devices located within the host computer, as well as to control devices located upon a distributed network.

FIG. 1 shows the principle components of a reconfigurable hardware system **11** in accordance with a preferred embodiment of the invention. The systems comprise a field programmable gate array (gate array) **13**, a random access memory **15**, a processor **17**, a configuration memory **19**, and a dedicated I/O port **31**. The processor **17** accesses the configuration memory **19**, field programmable gate array **13**, the random access memory **15**, and the I/O port **31**, all over data bus **27**. In one embodiment of the invention, the processor **17** and the random access memory **15** may be implemented as a single digital signal processor **21**. Alternatively, the processor **17** may be a suitable controller. In preferred embodiments, the system **11** will be installed within a host computer system **25** having a PCI bus **31**, and communication with the system will be through a data connection **29** linking the system **11** to the PCI bus. In a preferred embodiment of the invention, the components **11** will be manufactured as part of an expansion card to be plugged directly into a PCI expansion slot within the host computer **25**. In the expansion-card embodiment, the communication path **29** will be through the edge connectors of the expansion card within the PCI expansion slot.

In practice, the embodiment of FIG. 1 is used to perform real-time control of one or more devices attached to the embodiment. In preferred embodiments, there will be a direct

connection between the field programmable gate array **13** and a dedicated I/O port **31**. The dedicated I/O port will allow the gate array to control devices **41** directly attached to the invention, as well as to communicate through a data network **23** to control computers **33, 35** or other devices **37** located remotely from the invention. Since in preferred embodiments the gate array has its own dedicated I/O port, the invention will be able to communicate and control devices in a manner independent of and parallel to the operation of the host computer.

In order for real-time control to be feasible, preferred embodiments of the invention will require that for controlling more than a few simple devices, or if controlling devices located far from the invention, that the network **23** be a high-speed network having a data throughput of at least 200 Megabit/sec. In addition, the network should have guaranteed latencies that are sufficiently depending on the application. A suitable network, for example, may be operate din accordance with IEEE standard P1394, which is marketed commercially by licensees of Apple Computer Systems of Cupertino California, under the FIREWIRE trademark. For a device **41** attached directly to the invention, a low-speed fiber-optic connection may be utilized for communication to the invention. For remote devices and computers, preferred embodiments will have a hub **43** at the remote site for coordinating communication with the invention over the high-speed network **23**. For a device **37** or computers **33, 35** attached to the high-speed network **23** via the hub **43**, lower speed fiber-optic connections **39** may be utilized. The basic issue for all methods of connecting to the embodiment and thereby to the field programmable gate array **13** is to ensure that there is sufficient bandwidth over the lower speed fiber-optic connections **39** to allow for real-time control of attached devices, as well as sufficient bandwidth over the high-speed network **23** for carrying all of the control data back to the gate array **13**.

A simpler preferred embodiment of the invention may be used to control remote devices over low cost plastic optical fiber. When the low cost plastic optical fiber is insufficient to meet the communication needs of the attached devices, or when the distance between the devices and the controlling host computer are too long to allow use of low cost plastic optical fiber, a more sophisticated embodiment of the invention may be used. In this embodiment, a high-speed network link is used to attach the host computer to a hub located at a remote location, from which the low cost plastic optical fiber may then be used to connect to the hub devices that use local to it. In preferred embodiments, hubs may also be daisy-

chained via the high-speed communication links, so that devices very distant from the host computer may still be controlled. That is, hubs may be used to connect several distance-limited high-speed links. Embodiments of the present invention may support such topologies and embodiments are designed to allow for controlling devices in a fully distributed environment over wide area networks (WANS).

In preferred embodiments, the state of the field programmable gate array remains constant as long as power is applied to the gate array's circuitry. Therefore, during power-on of the host computer, which preferably supplies power to the embodiment, the embodiment will automatically test and reset the gate array to a known start state. In a preferred embodiment, a specialized software compiler is provided to convert a computer program into instructions suitable for programming the state of the gate array. The programming language may be C, C++ or some other high-level programming language. Through the specialized software, the gate array is programmed to perform a specific hardware function that would otherwise have been executed much more slowly in software. In addition, the gate array may itself be programmed to reprogram itself (in whole or in part) without further intervention depending on conditions experience in the course of control. This self-reprogramming could be due to the gate array's **13** presently loaded hardware configuration, or in response to an action performed by a device under control.

Programming the field programmable gate array **13** is achieved by sending the gate array a configuration signal. In response to this signal, the gate array's internal gates are set according to the contents of the configuration memory **19**. After the contents of the configuration memory **19** have been loaded, the gate array **13** now has a new hardware configuration. In a preferred embodiment, there will be little or no interaction between the host computer **25** and the embodiment, and thereby little drain upon the host's resources, except for programming the gate array into a new hardware configuration. In a further embodiment of the invention, there is provided a digital signal processor **21** (DSP) having its own central processing unit **17** and random access memory **15** local to the DSP, so that the DSP can act as a parallel processor for the host computer **25** and coordinate and control the programming of the gate array **13**.

In a further embodiment, in addition to receiving hardware configuration data from the configuration memory **19**, the field programmable gate array may also retrieve

configuration data from remote network locations. such as from remote computers **33, 35**, or from remote world wide web sites.

In two preferred embodiments of remote interface modules, the first embodiment has one acquisition and one interface card. The interface card provides the configuration/control support. a digital I/O port, and a low bandwidth optical link interface. The acquisition card provides two 16-bit A/D converters and 16 channels with programmable gains. There are also two additional true differential high-impedance channels: The maximum sampling rate for each channel is 200k samples per second. A second embodiment has the same characteristics as the first model except that an additional card is provided. This additional card provides 16 18-bit D/A channels in voltage mode and two additional channels with voltage or current outputs. A Digital Signal Processing (DSP) card is also available. which provides 40 or 50 MFLOPS (million floating point operations/sec). and several DSP cards can be installed within a hub when distributed computing power is required at the remote sites.

What is claimed is:

1. A dynamically reconfigurable hardware system for real-time control of an external device comprising:

(a) a configuration memory for storing a hardware configuration;

(b) a reconfigurable logic module, in communication with the configuration memory, for establishing the hardware configuration in the module on receipt of a configuration signal;

(c) a controller in communication over a data bus with reconfigurable logic module and the configuration memory for sending the configuration signal to the reconfigurable logic module and for establishing the hardware configuration in the configuration memory; and

(d) a communication port coupled to the reconfigurable logic module independently of signals on the data bus for controlling the external device;

2. A hardware system as described in claim 1, wherein the configuration memory is dual-ported random access memory.

3. A hardware system according to claim 1, wherein the configuration memory is electrically erasable programmable read only memory.

4. A hardware system according to claim 1, wherein the data bus is in communication with a network.

5. A hardware system according to claim 1, further comprising:

(e) a network, wherein the controller is in communication a network, and at least a portion of the hardware configuration is retrievable from a remote location on the network.

6. A hardware system according to claim 1, further comprising:

(e) a computer having a central processing unit in communication with the data bus;

(f) a graphics display for a user interface; and

(g) a process executing on the central processing unit that sends user interface data to the display, wherein the reconfigurable logic module performs computations in parallel with the process executing on the central processing unit.

7. A hardware system according to claim 6, wherein the network is the Internet, the user interface is an Internet browser, and wherein the browser retrieves at least a part of the

hardware configuration through the Internet.

8. A hardware system according to claim 1, wherein the system further comprises a digital signal processor that includes the controller.

9. A hardware system according to claim 4, wherein the network utilizes the IEEE P1394 protocol.

10. A method for controlling an external device in red time comprising:

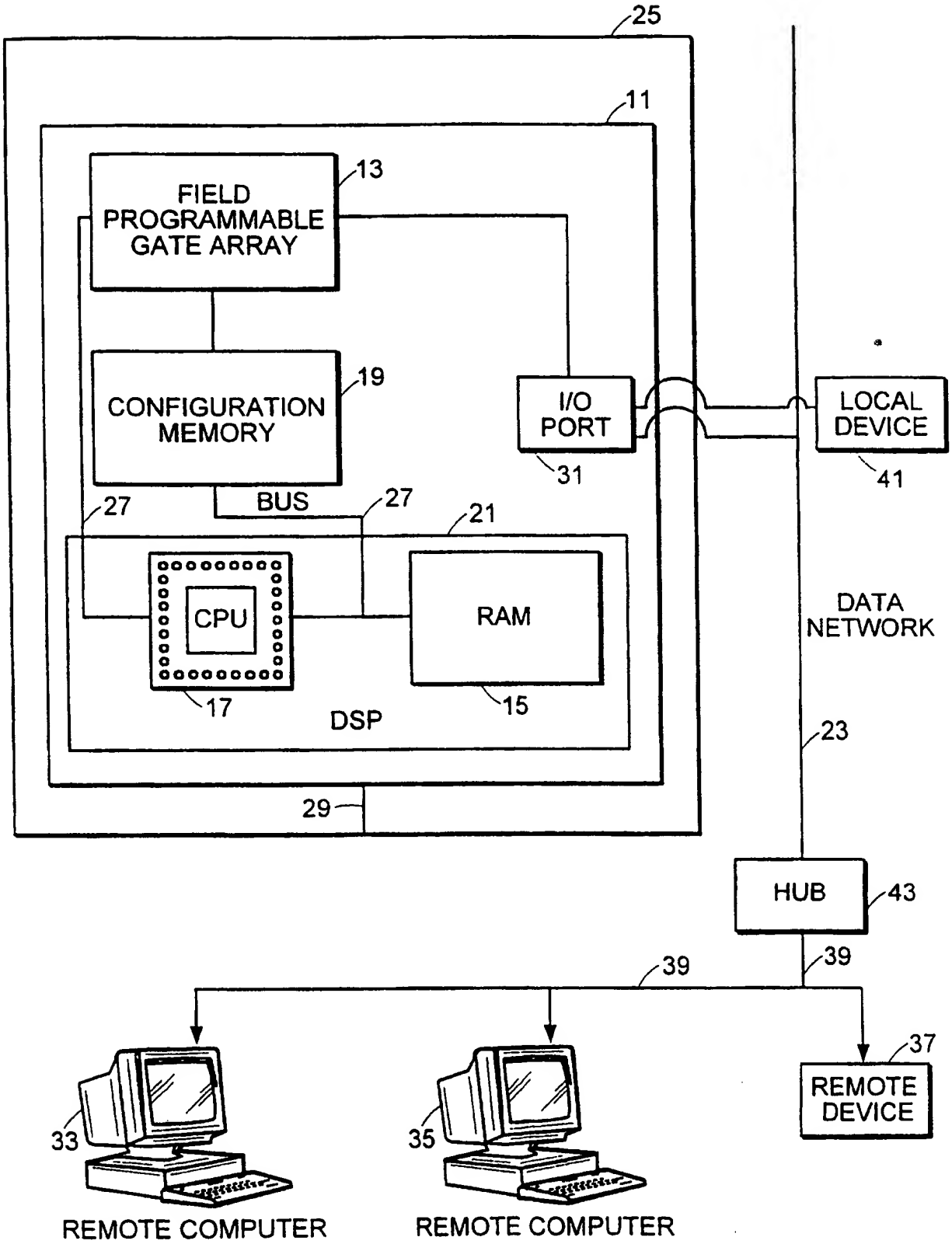
(a) storing a hardware configuration in a configuration memory:

(b) providing a reconfigurable logic module in communication with the configuration memory for establishing the hardware configuration in the module;

(c) establishing the hardware configuration in the reconfigurable logic module: and

(d) utilizing the reconfigurable logic module to control the external device.

11. A method according to claim 10, wherein step (e) includes providing at least a portion of the hardware configuration to the reconfigurable logic module over a network.


25
11
FIELD PROGRAMMABLE GATE ARRAY
13
CONFIGURATION MEMORY
19
I/O PORT
31
LOCAL DEVICE
41
BUS
27
27
21
CPU
17
RAM
15
DSP
DATA NETWORK
23
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HUB
43
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REMOTE DEVICE
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REMOTE COMPUTER
REMOTE COMPUTER

FIG. 1

INTERNATIONAL SEARCH REPORT

Inter. nal Application No
PCT/US 97/10763

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 G06F15/78

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	LECURIEUX-LAFAYETTE G: "UN SEUL FPGA DOPE LETRAITEMENT D'IMAGES" ELECTRONIQUE, no. 55, 1 January 1996, pages 98, 101-103, XP000551946 see the whole document --- -/--	1,3,6,10

[X] Further documents are listed in the continuation of box C.

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INTERNATIONAL SEARCH REPORT

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	WOODWARD D R ET AL: "An FPGA based configurable I/O system for AC drive controllers" PROCEEDINGS IEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS (CAT. NO.94CH35712), PROCEEDINGS 1994 IEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS AND PROCESSORS, CAMBRIDGE, MA, USA, 10-12 OCT. 19, ISBN 0-8186-6565-3, 1994, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC. PRESS, USA, pages 424-427, XP000488926 see page 425, right-hand column, line 13 - page 427, right-hand column, line 20 ---	1,10
A	PAGE I: "RECONFIGURABLE PROCESSOR ARCHITECTURES" MICROPROCESSORS AND MICROSYSTEMS, vol. 20, no. 3, 1 May 1996, pages 185-196, XP000590930 see the whole document ---	1,10
A	LIPMAN J: "MUC CHIP PROGRAM LETS YOU CHOOSE PREDEFINED OR CUSTOM CORE" EDN ELECTRICAL DESIGN NEWS, vol. 40, no. 16, 3 August 1995, page 21/22 XP000526551 see the whole document ---	1,2,10
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Information on patent family members

Interr. .nal Application No
PCT/US 97/10763

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
US 5289580 A	22-02-94	NONE	